IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A processor comprising:

a processor core including a general-purpose register, an instruction decoder, and a second execution unit;

an extension unit including a first execution unit connected to the processor core; and

a direct memory access controller connected to both the processor core and the extension unit.

2. (Original) The processor of claim 1, further comprising a control bus connected to the processor core and the extension unit.

3. (Currently Amended) The processor of claim 2, further comprising a clock disable signal generation circuit organized to receive an extended instruction code from the instruction decoder and ~~outputs~~ output a clock disable signal.

4. (Currently Amended) The processor of claim 3, further comprising a clock gating circuit organized to receive the clock disable signal and ~~transmits~~ transmit a signal for halting a clock signal for the processor core.

5. (Currently Amended) The processor of claim [[4]] 3, wherein the clock disable signal halts the clock signal for the processor core.

6. (Original) The processor of claim 2, further comprising a halt request signal generation circuit organized to receive an extended instruction code from the instruction decoder and transmit a halt request signal to the processor core.

7. (Original) The processor of claim 2, wherein the first execution unit is a reconfigurable first execution unit.

8. (Original) The processor of claim 7, wherein the extension unit further comprises an instruction decoder, a control register, and local memory.

9. (Original) The processor of claim 7, wherein the instruction decoder in the extension unit further comprises a reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

10. (Original) The processor of claim 7, wherein configuration data provided to the reconfigurable logic circuit, is provided through data transmission from the direct access memory controller via a configuration interface connecting the reconfigurable first execution unit in the extension unit and the direct memory access controller.

11. (Currently Amended) The processor of claim 8, wherein configuration data provided to the reconfigurable logic circuit is stored in the ~~internal~~ local memory of the extension unit.

12. (Original) A semiconductor integrated circuit, comprising:

a semiconductor chip;

a processor core integrated on the semiconductor chip including a general purpose register, an instruction decoder, and a second execution unit;

an extension unit integrated on the semiconductor chip including a first execution unit connected to the processor core;

a direct memory access controller integrated on the semiconductor chip and connected to both the processor core and the extension unit.

13. (Original) The semiconductor integrated circuit of claim 12, further comprising a control bus integrated on the semiconductor chip and connected to both the processor core and the extension unit.

14. (Currently Amended) The semiconductor integrated circuit of claim 13, further comprising a clock disable signal generation circuit integrated on the semiconductor chip and [[is]] organized to receive an extended instruction code from the instruction decoder and ~~outputs~~ output a clock disable signal.

15. (Currently Amended) The semiconductor integrated circuit of claim 14, further comprising a clock gating circuit integrated on the semiconductor chip and [[is]] organized to receive the clock disable signal and ~~transmits~~ transmit a signal for halting a clock for the processor core to the processor core.

16. (Currently Amended) The semiconductor integrated circuit of claim 13, further comprising a halt request signal generation circuit integrated on the semiconductor chip and [[is]] organized to receive an extended instruction code from the instruction decoder and transmit a halt request signal to the processor core.

17. (Original) The semiconductor integrated circuit of claim 13, wherein the first execution unit is a reconfigurable first execution unit.

18. (Original) The semiconductor integrated circuit of claim 17, wherein the instruction decoder in the extension unit further comprises a reconfigurable logic circuit that is the same as the reconfigurable first execution unit.

19. (Currently Amended) The semiconductor integrated circuit of claim [[17]] 18, wherein configuration data provided to the reconfigurable logic circuit, is provided through data transmission from the direct access memory controller via a configuration interface connecting between the reconfigurable first execution unit in the extension unit and the direct memory access controller.

20. (Currently Amended) The semiconductor integrated circuit of claim [[17]] 18, wherein configuration data provided to the reconfigurable logic circuit is stored in [[the]] internal local memory of the extension unit.